ABSTRACT

Disclosed here is a method for speeding up data writing and reducing power consumption by reducing the variation of the threshold voltage of each of non-volatile memory cells at data writing. When writing data in a memory cell, a voltage of about 8V is applied to the memory gate line, a voltage of about 5V is applied to the source line, a voltage of about 1.5V is applied to the selected gate line respectively. At that time, in the writing circuit, the writing pulse is 0, the writing latch output a High signal, and a NAND-circuit outputs a Low signal. And, a constant current of about 1ìA flows in a constant current source transistor and the bit line is discharged by a constant current of about 1ìA to flow a current in the memory cell.